

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **61117858 A**

(43) Date of publication of application: **05.06.86**

(51) Int. Cl.

H01L 25/08

(21) Application number: **59238387**

(71) Applicant: **HITACHI MICRO COMPUT ENG
LTD HITACHI LTD**

(22) Date of filing: **14.11.84**

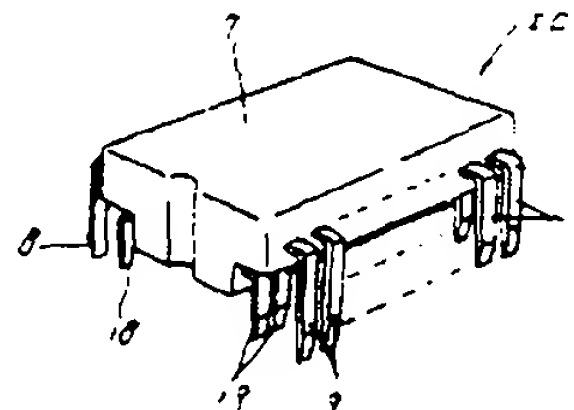
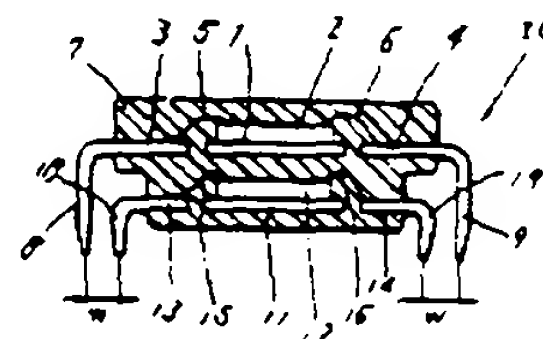
(72) Inventor: **TAKAHASHI HIDEKAZU**

(54) SEMICONDUCTOR DEVICE

(57) Abstract:

PURPOSE: To obtain a function of a plurality of ICs with one IC area by a method wherein semiconductor chips are provided in a stack in the same package.

CONSTITUTION: A semiconductor chip 2 is provided on the tab 1 of the upper stage, and the terminals of the chips 2 are bonded to the tips of inner leads 3, 4 with Au wires 5, 6 or the like. A semiconductor chip 12 is provided on the tab 11 of the lower stage, and the terminals of the chip 12 are bonded to the tips of inner leads 13, 14 with Au wires 15, 16 or the like. The other ends of the inner leads are outer leads 8, 9, 18, 19. Providing the semiconductor chips 2, 12 in the same package 17 not only makes double integration degrees but also enables mounting as one IC. The semiconductor chips may have either the same function or different functions in the same manner as the digital IC and the analog IC. Thus, the mounting area can be substantially reduced largely.



COPYRIGHT. (C)1986.JPO&Japio